RFL Industries, Inc., Boonton, New Jersey 07005

Model 66A MCOS
8 POINT MOMENTARY COS CARD

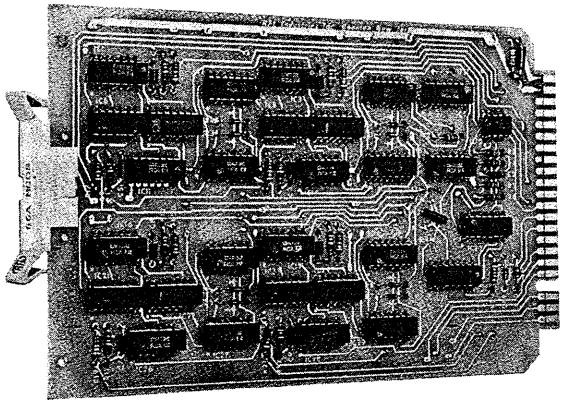


Figure 1. Model 66A MCOS 8-Point Momentary COS Card.

DESCRIPTION

Model 66A MCOS is one of the RFL 66 TDMS Series of plug-in logic cards. It will retain changes of state which occur at any of the eight status inputs for 1, 2, 3, or 4 counts of the clock input depending upon programming; after which it will output the then-current data. This card is particularly useful in applications where it is desirable to capture transient status conditions which last for very short times.

SPECIFICATIONS

No. of Inputs: 8.

Transient Time: 66A MCOS will recognize changes of state which last longer than 1 mS.

Ambient Temperature: −30 to +70°C.

Power: 11 to 13 Vdc at 13 mA.

Size: One standard one-half-inch module space in an RFL Model 68 Chassis.

PROGRAMMING AND CONNECTION

This module contains CMOS logic circuits and special handling precautions should be observed. Refer to "Semiconductor Handling Precautions", RFL Document 12175.

All unused input terminals or unused inputs to integrated circuits must be returned to +V or circuit common.

A change is retained for whatever number of counts is programmed by the M jumpers. See Figure 2. M1 = 1 count, M2 = two, M3 = three and M4 = four counts.

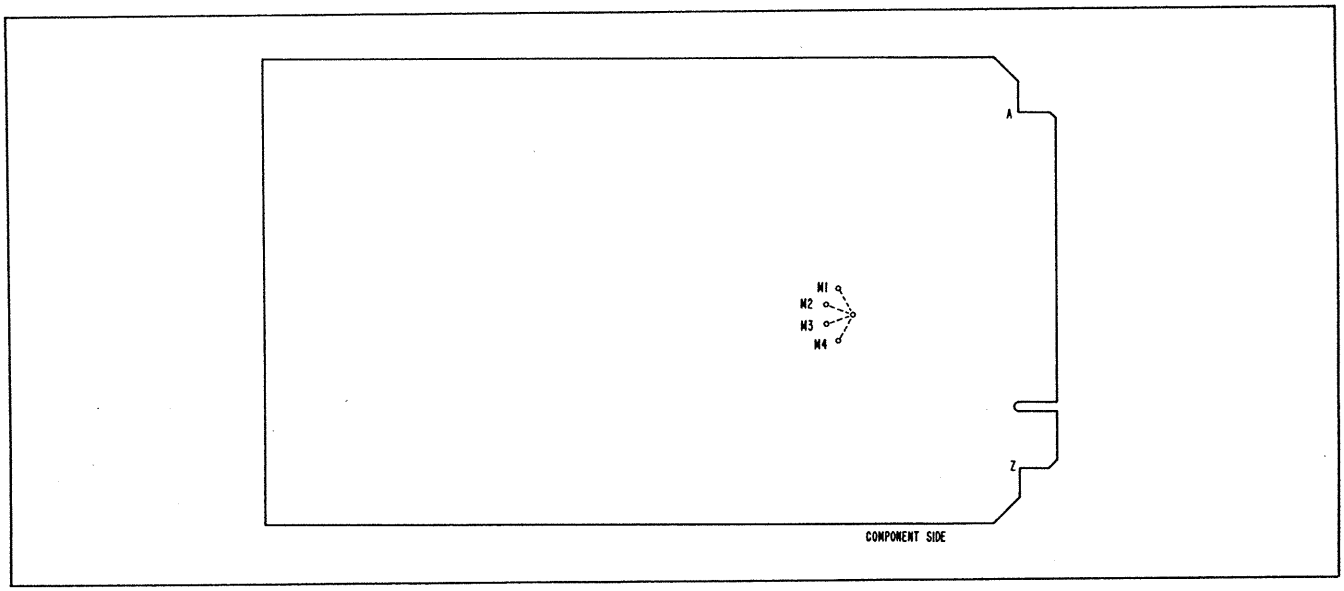


Figure 2. Location of jumpers for programming the number of messages sent for each change of state.

8–PT MOMENTARY COS CARD					
Module Designation	HB-44380	HB-44186 Option Pull-Up Resistor Set			
66A MCOS	•				
66A MCOS-1	•	•			

THEORY OF OPERATION

Figure 3 shows the timing of five examples for which it is assumed that the M3 jumper is installed.

The status output in Example 1 is the same as without memory. Example 2 and Example 3 show how transient status is retained for three clock pulses.

Example 4 shows what happens if the input state is different immediately after three counts, which themselves occurred after a change of state. Note the logic-0 input status during the fourth clock pulse. It too is treated as a change of status and causes the retain feature to be activated.

Example 5 indicates that the retained status will be extended by three counts if a second input on the same card has a change of status.

The logic associated with the #1 input at Terminal 4 (Figure 5, Zone A1) will be described. The logic for the other seven inputs functions in an identical manner.

Circuit operation depends upon the sequenced clock signals originating from IC5 (G1) and shown in Figure 4. IC10 (H1) and IC20A (H1) are wired to form a 12-kHz oscillator which drives IC5.

Assuming no changes of status have taken place for a long time, both inputs to IC9B (E1) will be 0, and hence so will IC8B-5 (D2). IC8B-6 drops low at the beginning of t_4 because it is connected to IC5-12, and this, in turn, clocks the D-type flip-flop IC13A (C1). Thus, the input status is transferred to IC13A-1 at the start of t_4. This status is available to the edge connector Terminal 21. As long as the status is never changed, everything is normal and IC13B (C1), IC14A (D1) and IC14B (E1) are in a set condition; that is, they all have logic ones at their Q outputs.

If a change of status does occur at the input, the new status and its complement will be available at the Q and $\overline{Q}$ outputs of IC13A when the beginning of the next t_4 time period occurs. If the status changed from a 0 to a 1, IC13A-1 will go high and clock IC13B; but if the status changed from a 1 to a 0, IC13A-2 will go high and clock IC14A. One or the other change-detector flip-flop will cause a zero at an input to IC9A (D1) and force its output at Pin 3 to a one.

A one at IC9A-3 enables gate IC9B which, as will be shown later, prevents any further clocking of IC13A. However, when IC9A-3 first goes high, the 0 at the D input of IC14B is transferred to IC14B-13. This Q output is ORed through CR1 to pull down the voltage at the D input of IC15B (G3). Thus IC15B-9 will be low within several propagation delays after t_4 if any input has changed.

At t_6 IC15B is clocked, and if there is a 0 at pin 9, then pin 12, $\overline{Q}$, will go high. This high sets IC14B again, and it also resets IC25B (H3). At t_7 IC15B is itself set again.

IC25 is a 4-bit serial-in-parallel-out shift register. Because of the pulse from IC15B, all of the Q out-

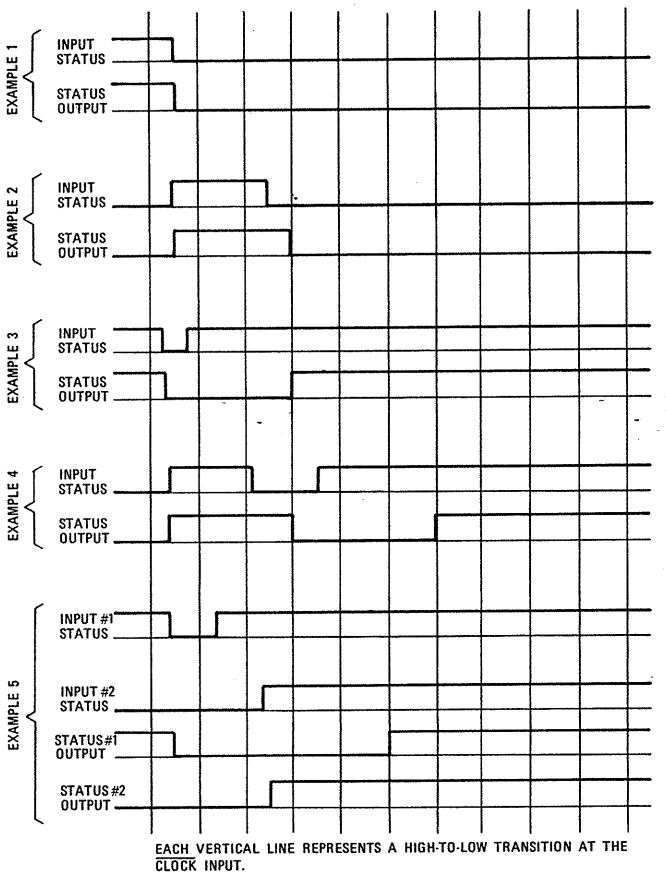


Figure 3. Timing diagram for examples discussed in text.

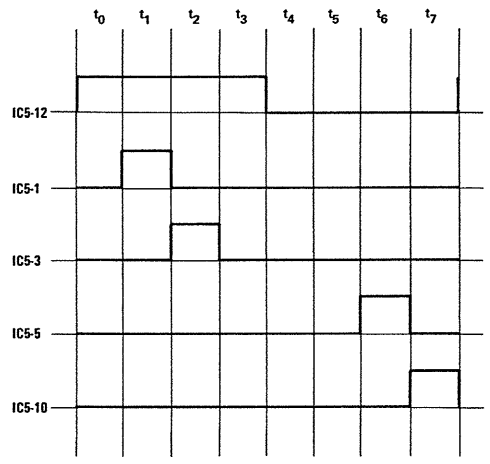


Figure 4. Clock-time sequencing.

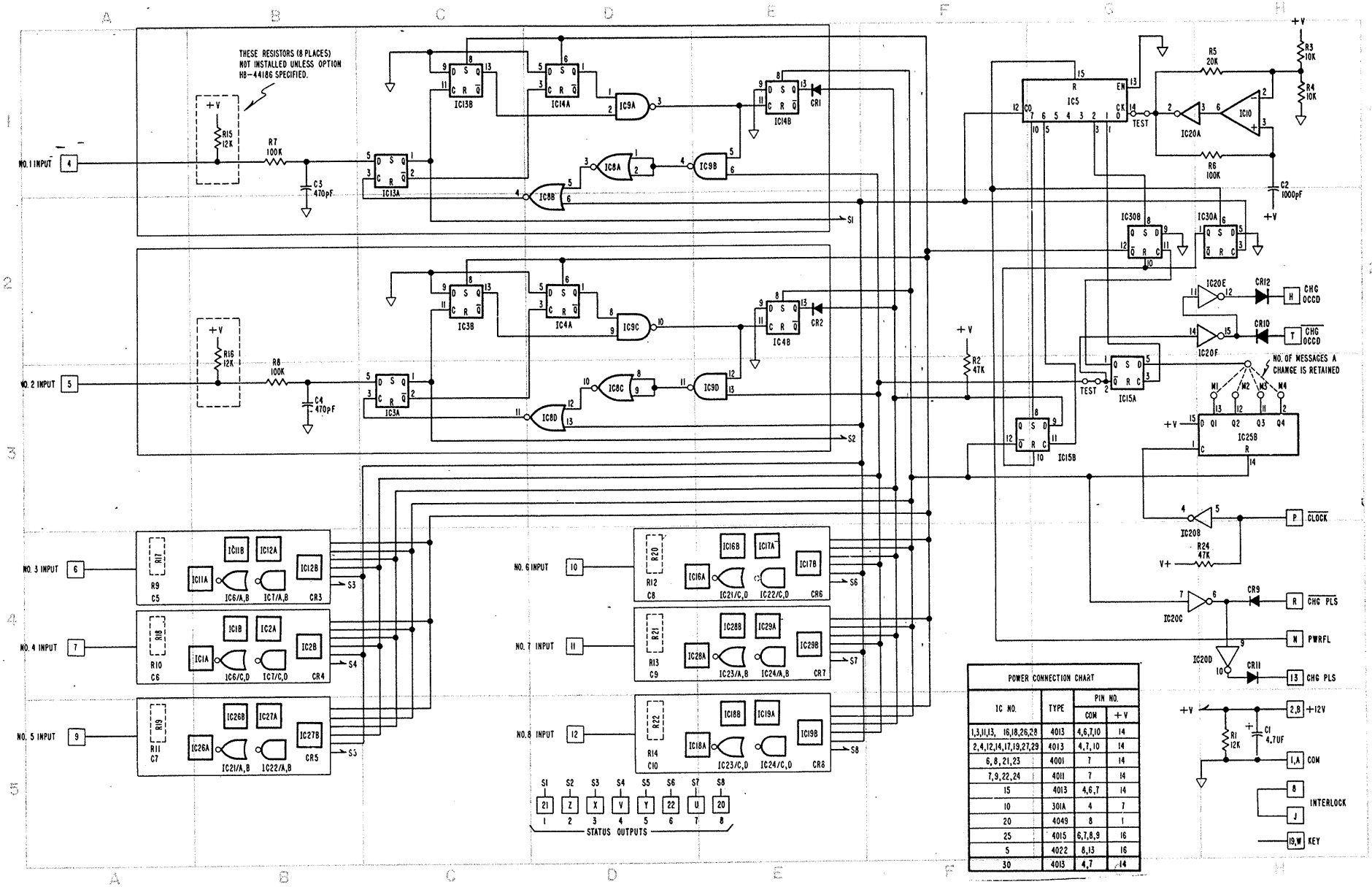
puts of IC25B (H3) are at a logic 0. These outputs will remain 0 until a 1 can be shifted in by the proper number of $\overline{\text{CLOCK}}$ pulses. IC25B was reset during t_6. IC15A (G3) is clocked at the beginning of t_1, at which time its Q goes to a 1. The state of IC15A's outputs will also stay fixed until a programmed Q output from IC25B changes to a 1.

Because IC15A-2 is in the 1 state, IC9B-6 (E1) will be high. IC9B-5 also has a high as a result of the changed input status at Terminal 4. IC9B-4 will be low and IC8A-3 (D1) will be high. Thus the clocking of IC13A (C1) is prevented because IC8B's output is forced to a low continuously.

Eventually, the proper number of counts will have been inputted, and IC15A-5 will go high. At the start of t_1, IC15A-2 drops low to allow clocking the input flip-flop IC13A via IC9B, IC8A and IC8B. When IC15A-2 went low, IC15A-1 went high, and this action clocked the 1 at IC25A-7 (H2) into IC25A's Q1 output. IC25A is used as a monostable since it is reset at the beginning of the next time period, t_2. The pulse from IC25A-5 sets the change detector flip-flops IC13B and IC14A, which in turn forces IC9A-3 low again. The logic is again in its initial condition and ready to clock status into IC13A at the leading edge of t_4.

PARTS LIST

CIRCUIT SYMBOL	DESCRIPTION	PART NUMBER
R1-14	Resistor, fixed, composition, ¼W, 5%, value on schematic, Allen Bradley CB, or eq.	H-1009-(XXX)
R15-23	Optional pull-up resistors, 12K, 5%, ¼W, fixed, composition, Allen Bradley CB, or eq.	H-1009-805
C1	Capacitor, tantalum, 4.7μF, 20%, 20V, Kemet T324B475M020AS, or eq.	H-1007-711
C2	Capacitor, ceramic, 1000pF, 10% 100V, Union Carbide CK12, or eq.	H-1007-1360
C3-10	Capacitor, ceramic, 470pF, 10%, 100V, Union Carbide CK12, or eq.	H-1007-1358
CR1-11	Diode, Type 1N914B	HA-26482
IC1-4, 11-19, 26-29	Dual, D-Type, flip-flop, RCA CD4013AE, or eq.	H-0615-1
IC5	Divide-by-8 Counter/Divider, RCA CD4022AE, or eq.	H-0615-6
IC6, 8, 21, 23	Quad, 2-input, NOR gate, RCA CD4001AE, or eq.	H-0615-3
IC7, 9, 22, 24	Quad, 2-input, NAND gate, RCA CD4011AE, or eq.	H-0615-5
IC10	Operational amplifier, National LM301A, or eq.	H-0620-76
IC20	Hex Inverter, buffer RCA CD4049AE, or eq.	H-0615-7
IC25	Dual, 4-stage shift register, RCA CD4015AE, or eq.	H-0615-25
	Shorting bar	HA-42904
	Schematic	HE-44384



POWER CONNECTION CHART			
IC NO.	TYPE	PIN NO.	
		COM	+V
1,3,11,13, 16,18,26,28	4013	4,6,7,10	14
2,4,12,14,17,19,27,29	4013	4,7,10	14
6,8,21,23	4001	7	14
7,9,22,24	4011	7	14
15	4013	4,6,7	14
10	301A	4	7
20	4049	8	1
25	4015	6,7,8,9	16
5	4022	8,13	16
30	4013	4,7	14

Figure 5. Schematic of circuit, Model 66A MCOS.